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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/534,903	05/16/2005	Ramkrishnan Venkata Subramanian	1890-0248	2393

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EXAMINER	
PARK, JEONG S	

ART UNIT	PAPER NUMBER
2454	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/534,903	VENKATA SUBRAMANIAN ET AL.	
	Examiner	Art Unit	
	JEONG S. PARK	2454	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to Application No. 10/534,903 filed on 5/16/2005. The argument presented on 2/23/2009 is hereby acknowledged. Claims 9-28 have been examined.

Claim Objections

2. Claims 17-20 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. There is no claim 96 within the present amendment.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 9, 11-16, 18-21 and 23-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bolan al. (hereinafter Bolan)(U.S. Patent No. 5,210,828), and further in view of Wu (U.S. Patent No. 6,151,644), and further in view of Juri et al. (hereinafter Juri)(EP Pub. No. 0599257 A2).

Regarding claims 9, 21 and 25, Bolan teaches as follows:

A mailbox apparatus or a method (interprocessor communication facility 50 contains arbitration circuitry 60, mailbox circuitry 100 and processor interrupt circuitry

100 in figure 1, see, e.g., col. 3, lines 56-58) for temporally storing messages (mailbox circuitry receives message from sending processors and provides them to the intended receiving processors, see, e.g., col. 5, lines 6-9), each message including a sequence of one or more data packets being transferred between a plurality of locations (segmentation is inherent for large message size depending on the bus transferring capability), the mailbox apparatus (interprocessor communication facility, 50 in figure 1 and 2) including a main memory (holding register, 61-63 in figure 2), an ancillary memory (mailbox array 105 and message output register 160 in figure 2)(see, e.g., col. 5, lines 6-16 and figure 2), and a control unit which is arranged to:

Receive a first message from one of the plurality of locations (arbitration circuitry, 60 in figure 2, decodes the commands sent from the processors through communication bus 41-43 and routes them either to processor interrupt circuitry or to mailbox circuitry, see, e.g., col. 3, line 67 to col. 4, line 4) without storing the first data packet in the main memory (the first data packet of the first message is inherently pass through the holding register (61-63 in figure 2, equivalent to applicant's main memory, see, e.g., col. 4, lines 5-19) and is stored at the mailbox entry because the mailbox entry for each processor is empty when the interprocessor communication facility (50 in figure 2, equivalent to applicant's mailbox apparatus) receives the first message);

Store at least a first data packet of the first message in the ancillary memory (mailbox array 105 and message output register 160 in figure 2) and at least one other data packet of the first message in the main memory (holding register, 61-63 in figure 2)(see, e.g., col. 6, lines 36-57); and

In response to a read signal (read message commend), transmit the first data packet of the first message from the ancillary memory to another location (message output register sends the message to the processor who issued the read commend), replenish the ancillary memory by transferring at least one of the at least one other data packet of the first message to the ancillary memory from the main memory (message is retrieved from the addressed mailbox entry and placed in message output register)(see, e.g., col. 6, lines 48-57) and transmit that the at least one of the at least one other data packet of the first message from the ancillary memory to another location (when the message is retrieved from the addressed mailbox entry the message is placed in message output register (160 in figure 2) to transmit to the other processor (20 in figure 2), see, e.g., col. 6, lines 48-57).

Wu further teaches as follows:

A buffer memory (18 in figure 2) consists of a set of uniform sized packet buffers (interpreted as multiple memories) which are subdivided into a set of smaller packet cells of uniform size (see, e.g., abstract);

Packet buffer (10 in figure 1) receives and stores data packets arriving sequentially on a network bus and then forwards them outward on another network bus in the order received (packet buffer temporally stores sequence of packets being transferred between a plurality of locations, see, e.g., col. 3, lines 25-37); and

When receive module receives a large packet, which is larger than can be stored in a single packet buffer, it reserves the next unoccupied packet buffer, wherein the packet buffer PB0 is interpreted as applicant's ancillary memory and packet buffer PB1

as the main memory (see, e.g., col. 4, lines 30-63).

Therefore the first portion of the large packet is stored at the packet buffer PB0 (equivalent to applicant's ancillary memory) and the rest of the large packet are stored at the packet buffer PB1-PBN (equivalent to applicant's main memory).

It would have been obvious for one of ordinary skill in the art at the time of the invention to modify Bolan to include a plurality of packet buffers as taught by Wu in order to efficiently transfer sequence of packets between input and output buses.

Bolan in view of Wu do not teach the main memory and the ancillary memory are of different type.

Juri teaches as follows:

Sending and storing data blocks (equivalent to applicant's first message) to a first memory means (7 in figure 4, equivalent to applicant's ancillary memory)(see, e.g., col. 2, lines 36-40);

Sending overflow data of the data blocks (equivalent to applicant's at least one other data packet of the first message) that has overflown from an allocated memory area (applicant's ancillary memory) for storing the overflow data in a second memory means (8 in figure 4, equivalent to applicant's main memory)(see, e.g., col. 2, lines 43-46); and

Transferring overflow data stored in the second memory means to the vacant area in the first memory means (see, e.g., col. 2, lines 46-49).

It would have been obvious for one of ordinary skill in the art at the time of the invention to modify Bolan in view of Wu to include an overflow memory as taught by Juri in order to efficiently process the data overflown from the main memory.

Regarding claims 11, 18 and 23, Bolan teaches as follows:

The ancillary memory (mailbox circuitry) is implemented as registers (message output register, see, e.g., col. 5, lines 10-12).

Regarding claims 12, 19, 24, 27 and 28, Bolan teaches as follows:

The control unit is further configured to transmit the stored data packet from the ancillary memory (message output register sends the message to the processor who issued the read commend) and replenish the ancillary memory (message is retrieved from the addressed mailbox entry and placed in message output register, see, e.g., col. 6, lines 48-57);

Four clock cycles to decode and execute a command (see, e.g., col. 5, lines 56-68);

Each mailbox portion (110, 120, and 130 in figure 2, equivalent to applicant's ancillary memory) contains one or more mailbox entries (see, e.g., col. 5, lines 16-18);

When the message is retrieved from the addressed mailbox entry the message is placed in message output register (160 in figure 2)(see, e.g., col. 6, lines 48-57); and

Since the mailbox portion has limited number of mailbox entries, the other data packets, which were waiting at the holding register, is inherently processed to the mailbox portion when the mailbox entry is empty (rock bit 151 in figure 4 is zero, see, e.g., col. 5, lines 33-38).

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the invention to process the replenishing function (receiving the other data packet from the holding register to the mailbox portion) together with transmitting the stored data packet from the ancillary memory (transmitting to the output register).

Regarding claims 13 and 20, Bolan teaches as follows:

The ancillary memory is configured to store a number of data packets which is at least equal to a number of clock periods required to extract any data packet from the main memory (four clock cycles to decode and execute a command, see, e.g., col. 5, lines 56-68, therefore each clock cycle completes one extraction of data packet from the main memory for write/read commands).

Regarding claim 14, Bolan teaches as follows:

A plurality of ancillary memories (mailbox portions, 110, 120 and 130 in figure 2), each ancillary memory having a distinct corresponding locations, each ancillary memory being arranged to store data packets to be transmitted to the corresponding location (mailbox array, 105 in figure 2, contains mailbox portions, which are reserved for the use of processors, 10, 20 and 30 in figure 2, see, e.g., col. 5, lines 12-18).

Regarding claim 15, Bolan teaches as follows:

Message field segment contains the beginning and ending of address of the task control block located in main storage, see, e.g., col. 5, lines 27-33).

It would have been obvious for one of ordinary skill in the art at the time of the invention to modify Bolan to include message segmentation in order to transfer large size of message beyond the capacity of bus between two processors into multiple of

proper packets.

Regarding claims 16 and 26, Bolan teaches as follows:

A plurality of processors or a method (10, 20 and 30 in figures 1 and 2) and a mailbox apparatus (interprocessor communication facility 50 contains arbitration circuitry 60, mailbox circuitry 100 and processor interrupt circuitry 100 in figure 1, see, e.g., col. 3, lines 56-58), a first processor (processor 10 in figure 2) of the plurality of processors being arranged to transfer a message to a second processor (processor 20 in figure 2) of the plurality of processors by transmitting the message as a series of data packets to the mailbox apparatus (mailbox circuitry 100 in figure 2) and sending a signal (interrupt signal) to the second processor to indicate the presence of the message in the mailbox apparatus (sends an interrupt to processor 20 indicating a synchronous message is in the mailbox waiting for processing, see, e.g., col. 9, lines 14-20), the second processor being arranged in response to send a read signal to the mailbox apparatus (processor 20 use a read message command to get the message, see, e.g., col. 9, lines 20-21)(synchronous message transaction between processor 10 to processor 20, see, e.g., col. 8, line 63 to col. 9, line 33);

The mail box apparatus comprising a main memory, an ancillary memory, and a control unit which is arranged to (see, e.g., col. 5, lines 6-16 and figure 2);

Receive the message from the first processor (arbitration circuitry, 60 in figure 2, decodes the commands sent from the processors through communication bus 41-43 and routes them either to processor interrupt circuitry or to mailbox circuitry, see, e.g., col. 3, line 67 to col. 4, line 4);

Store at least a first data packet of the message in the ancillary memory (mailbox array 105 and message output register 160 in figure 2) without storing the first data packet in the main memory (the first data packet of the first message is inherently pass through the holding register (61-63 in figure 2, equivalent to applicant's main memory, see, e.g., col. 4, lines 5-19) and is stored at the mailbox entry because the mailbox entry for each processor is empty when the interprocessor communication facility (50 in figure 2, equivalent to applicant's mailbox apparatus) receives the first message) and store at least one other data packet of the message in the main memory (holding register, 61-63 in figure 2)(see, e.g., col. 6, lines 36-57); and

In response to a read signal (read message commend), transmit the first data packet of the first message from the ancillary memory to another location (message output register sends the message to the processor who issued the read commend), replenish the ancillary memory by transferring at least one of the at least one other data packet of the first message to the ancillary memory from the main memory (message is retrieved from the addressed mailbox entry and placed in message output register)(see, e.g., col. 6, lines 48-57) and transmit that the at least one of the at least one other data packet of the first message from the ancillary memory to another location (when the message is retrieved from the addressed mailbox entry the message is placed in message output register (160 in figure 2) to transmit to the other processor (20 in figure 2), see, e.g., col. 6, lines 48-57).

Wu further teaches as follows:

A buffer memory (18 in figure 2) consists of a set of uniform sized packet buffers

(interpreted as multiple memories) which are subdivided into a set of smaller packet cells of uniform size (see, e.g., abstract);

Packet buffer (10 in figure 1) receives and stores data packets arriving sequentially on a network bus and then forwards them outward on another network bus in the order received (packet buffer temporally stores sequence of packets being transferred between a plurality of locations, see, e.g., col. 3, lines 25-37); and

When receive module receives a large packet, which is larger than can be stored in a single packet buffer, it reserves the next unoccupied packet buffer, wherein the packet buffer PB0 is interpreted as applicant's ancillary memory and packet buffer PB1 as the main memory (see, e.g., col. 4, lines 30-63).

Therefore the first portion of the large packet is stored at the packet buffer PB0 (equivalent to applicant's ancillary memory) and the rest of the large packet are stored at the packet buffer PB1-PBN (equivalent to applicant's main memory).

It would have been obvious for one of ordinary skill in the art at the time of the invention to modify Bolan to include a plurality of packet buffers as taught by Wu in order to efficiently transfer sequence of packets between input and output buses.

Bolan in view of Wu do not teach the main memory and the ancillary memory are of different type.

Juri teaches as follows:

Sending and storing data blocks (equivalent to applicant's first message) to a first memory means (7 in figure 4, equivalent to applicant's ancillary memory)(see, e.g., col. 2, lines 36-40);

Sending overflow data of the data blocks (equivalent to applicant's at least one other data packet of the first message) that has overflown from an allocated memory area (applicant's ancillary memory) for storing the overflow data in a second memory means (8 in figure 4, equivalent to applicant's main memory)(see, e.g., col. 2, lines 43-46); and

Transferring overflow data stored in the second memory means to the vacant area in the first memory means (see, e.g., col. 2, lines 46-49).

It would have been obvious for one of ordinary skill in the art at the time of the invention to modify Bolan in view of Wu to include an overflow memory as taught by Juri in order to efficiently process the data overflown from the main memory.

5. Claims 10, 17 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bolan al. (hereinafter Bolan)(U.S. Patent No. 5,210,828), Wu (U.S. Patent No. 6,151,644), and Juri et al. (hereinafter Juri)(EP Pub. No. 0599257 A2) as applied to claims 9, 16 and 21 above, and further in view of Ternes et al. (hereinafter Ternes)(U.S. Patent No. 4,935,894).

Regarding claims 10, 17 and 22, Bolan teaches all the limitations of claim except for teaching of using FIFO register as an ancillary memory.

Ternes teaches as follows:

Bus interface circuit (40 and 50 in figure 2) comprises a first-in-first-out (FIFO) register stack (55 and 60 in figure 2), interrupt logic, and transmitter/receiver logic. The pair of bus interface circuits provides dual simplex data and control transfer between the

two buses (see, e.g., col. 2, lines 46-50 and figure 2).

It would have been obvious for one of ordinary skill in the art at the time of the invention to modify Bolan to include FIFO register as a buffer memory as taught by Ternes in order to process multiple packets in sequence between two processors.

Response to Arguments

6. Applicant's arguments filed 2/23/2009 have been fully considered but they are not persuasive.

A. Summary of Applicant's Arguments

In the remarks, the applicant argues as followings:

Bolan in view of Wu and Juri does not teach a control unit which is arranged to store at least a first data packet of the first message in the ancillary memory without storing the first data packet in the main memory and store at least one other data packet of the first message in the main memory, wherein the main memory is of a first type, and the second memory is of a second type that is different than the first type.

B. Response to Arguments:

In response to argument, Bolan teaches as follows:

Mailbox circuitry receives message from sending processors and provides them to the intended receiving processors (see, e.g., col. 5, lines 6-9).

Bolan does not teach of storing a first data packet in one memory without storing the first data packet in the other memory and FIFO between two memories.

Wu teaches a process of storing a first data packet in one packet unit without storing the first data packet in the other packet unit and FIFO between two packet units as follows:

A buffer memory (18 in figure 2) consists of a set of uniform sized packet buffers (interpreted as multiple memories) which are subdivided into a set of smaller packet cells of uniform size (see, e.g., abstract);

Packet buffer (10 in figure 1) receives and stores data packets arriving sequentially on a network bus and then forwards them outward on another network bus in the order received (packet buffer temporally stores sequence of packets being transferred between a plurality of locations, see, e.g., col. 3, lines 25-37); and

When receive module receives a large packet, which is larger than can be stored in a single packet buffer, it reserves the next unoccupied packet buffer, wherein the packet buffer PB0 is interpreted as applicant's ancillary memory and packet buffer PB1 as the main memory (see, e.g., col. 4, lines 30-63).

Therefore the first portion of the large packet is stored at the packet buffer PB0 (equivalent to applicant's ancillary memory) and the rest of the large packet are stored at the packet buffer PB1-PBN (equivalent to applicant's main memory).

Bolan in view of Wu do not teach the main memory and the ancillary memory are of different type.

Juri teaches the deficiency of providing within two different memories as follows:

Sending and storing data blocks (equivalent to applicant's first message) to a first memory means (7 in figure 4, equivalent to applicant's ancillary memory)(see, e.g., col. 2, lines 36-40);

Sending overflow data of the data blocks (equivalent to applicant's at least one other data packet of the first message) that has overflown from an allocated memory area (applicant's ancillary memory) for storing the overflow data in a second memory means (8 in figure 4, equivalent to applicant's main memory)(see, e.g., col. 2, lines 43-46); and

Transferring overflow data stored in the second memory means to the vacant area in the first memory means (see, e.g., col. 2, lines 46-49).

The examiner interpreted the argued limitation as the well known FIFO process between two memories and parallel input to two memories and serial output from one memory to the other processor.

Therefore, Juri teaches the deficiency of Bolan in view of Wu by teaching FIFO process between first memory and second memory.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEONG S. PARK whose telephone number is (571)270-1597. The examiner can normally be reached on Monday through Friday 7:00 - 3:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. S. P./

Examiner, Art Unit 2454

May 5, 2009

/Nathan J. Flynn/
Supervisory Patent Examiner, Art Unit 2454